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A program to insert simulated synapses and
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A version of DYNCLAMP4 for two neurons.

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OPERATION MANUAL

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OPERATION MANUAL

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These are preliminary versions of the program, but they have been exhaustively used by us and proved to be functional and safe. However, there can be still some small problems, so if you find it useful we will really appreciate your feedback. We have a short paper in Journal of Neuroscience Methods 108 (2001) 39-48 describing the program and its use, so if you use it to make experiments you are going to publish somewhere, we would appreciate to see our work cited by you. Feel free to contact us for any further questions (reynaldo@ucsd.edu or reynaldo@fge.if.usp.br).

The authors.

INTRODUCTION:

The Dynamic Clamp protocol, developed by Sharp *et. al.* (*J. Neurophysiol.* **69**, 992-995, 1993) allows "insertion" of simulated membrane conductances in, and/or simulated synapses between biological neurons. Until now, the protocol has been applied simultaneously, at most, 2 neurons. Also, most commercial ADC/DAC boards (eg. Axon Instruments Digidata 1200/1300 series) possess only two analog outputs. Here we describe DYNCLAMP4, a method for controlling up to 4 neurons in real time, dynamic clamp mode.

- PC-based software permits up to 8 (or more) Hodgkin-Huxley conductances and up to 18 synaptic connections (chemical, non-rectifier electrical and rectifier electrical),
- An auxiliary electronic circuit splits the usual 2 analog outputs to 4 analog command signals.

We used a ADC/DAC DIGIDATA 1200A board from Axon Instruments, Inc., and using the auxiliary sample and hold circuit split the two analog outputs of the ADC/DAC board into four outputs we connected up to four neurons using the DYNCLAMP4. The program was written in C++ and runs in a Pentium III 450 MHz under Windows NT 4.0 but the program is also compatible with Windows 95/98/2000. The minimum update rate of the current using 4 neurons is of 5 kHz. A version for two neurons (DYNCLAMP2) which does not need auxiliary circuitry runs at 10 kHz.

HARDWARE AND SOFTWARE REQUIREMENTS:

- Pentium PC compatible computer ;
- Windows NT 4.0, 95, 98 or 2000;
- The Desktop Area in the Display Properties menu should be set to a minimum of 1152x864 pixels for running DYNCLAMP2 and to a minimum of 1280x1024 pixels for running DYNCLAMP4;
- DIGIDATA 1200A ADC/DAC board from Axon Instruments, Inc.;
- Analog demultiplex - described here (if you want to run DYNCLAMP4).

The programs were tested in a PC Compatible computer with a Pentium III 450MHz CPU and Windows NT 4.0 operational system. We suggest the use of Windows NT because it allows the control of the priority of the various programs running simultaneously and one can set the priority of the DYNCLAMP4 or DYNCLAMP2 to maximum, ensuring the program will generate accurate currents updated at very fast rates, but the other versions of windows are also possible.

ASYNCHRONOUS DYNAMIC CLAMP CYCLE:

The dynamic damp protocol consists in a cycle of reading the membrane potential of the cells, calculate the current to be injected in the cells through to all the synapses and conductances one wants to simulate, and to generate the voltage commands corresponding to these currents. This cycle should be repeated as fast as possible to simulate the continuous biological processes and the currents need to be calculated in real time according to the changes in the membrane potentials of the cells.

Since Windows is not a real time operating system, we will never know "a priori" exactly how long the digitalization of the membrane potentials, the calculation of the currents, and the generation of the command voltages will take. To solve these problem we made our program based in a asynchronous dynamic clamp cycle.

Every time the program updates the membrane potential of the cells it also reads the real time clock in the Digidata 1200A ADC/DAC board, so it knows exactly how long does it take between two successive updates. These time intervals between the updates are used in the dynamic computation of the currents and they not only allowed the implementation of the dynamic clamp protocol in the Windows environment but also made the program very flexible and optimized, since it can run faster if just a few synapses or conductances are implemented than if one have a loaded complex configuration with many different conductances and synapses.

TWO OR FOUR NEURONS?

We developed DYNCLAMP4 to connect up to four neurons, but for that purpose we needed to develop an analog demultiplex circuitry to generate four command voltages for the microelectrode amplifiers from the two analog outputs of the Digidata 1200A ADC/DAC board. If one doesn't need to connect more than two neurons we modified DYNCLAMP4 to obtain DYNCLAMP2 that doesn't need additional hardware (only the Digidata 1200A board) to connect two neurons.

ANALOG DEMULTIPLEX CIRCUIT FOR DYNCLAMP4:

We reproduce the schematics of the analog demultiplex used with DYNCLAMP4 in the Figure 1. The circuit consists basically of a sample and hold chip (SMP04) from Analog Devices Inc. and some circuitry for temporization and amplification.

Special care should be taken when building the analog demultiplex to avoid crossing wires used for logical levels with the wires in the input of the operational amplifiers and the sample and hold. The proximity between these wires can induce noise from the digital lines to

the analog ones. To solve these problem we displaced the various components in a physical configuration that allowed us to spatially isolate as much as we could the logical lines from the analog ones.

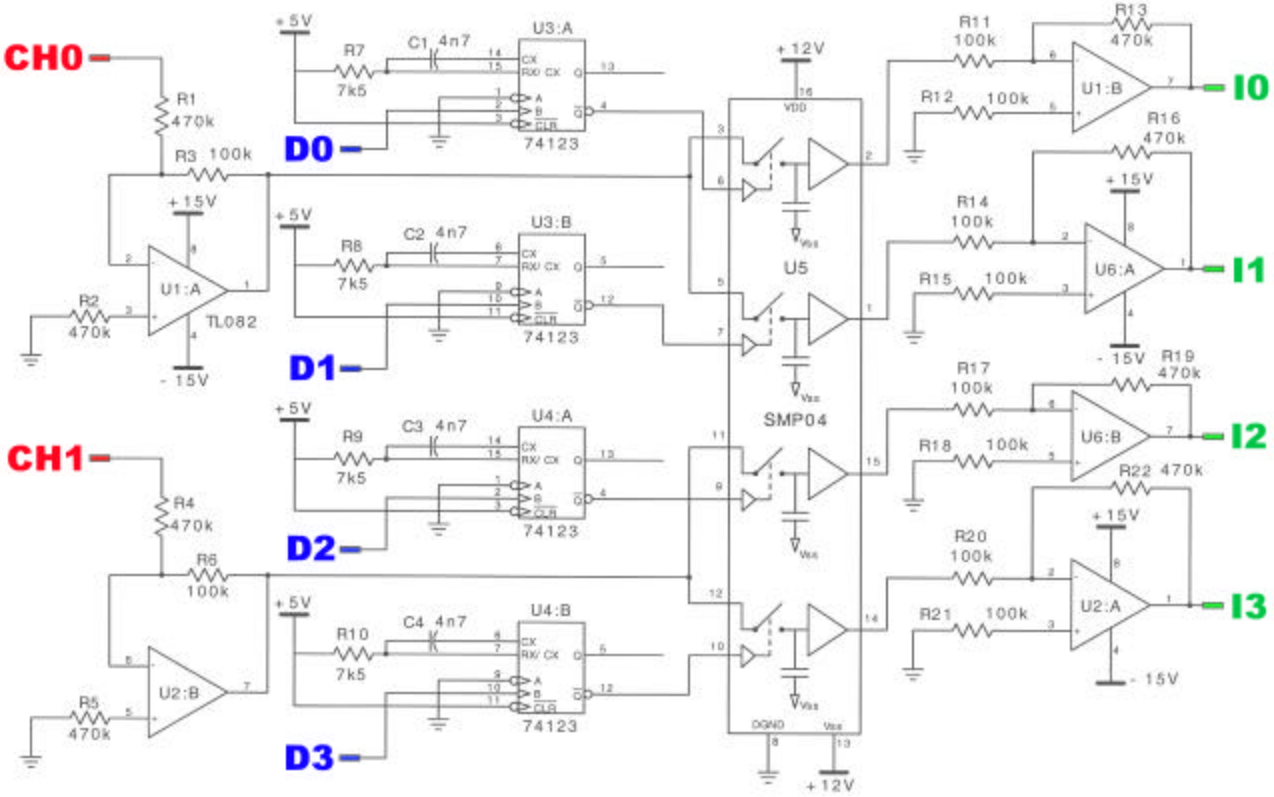

Figure 1. Schematic diagram of the analog demultiplex. The signals CH0 and CH1 correspond to the analog outputs of the ADC/DAC board, D0 - D3 are the first four digital outputs of the ADC/DAC board, and I0 - I3 are the outputs of the analog demultiplex that contains the encoded current to be injected in the neurons.

We used off the shelf components for building the circuit and these components usually have 5% tolerance in their values. To correct the effect of the limited precision of the components in the voltage gain and voltage offset of the analog demultiplex we included some calibrations in the parts of the DYNCLAMP4 program that generate the voltage commands for the currents. Once one builds an analog demultiplex like the described one the calibrations of the current should be redone by recompiling DYNCLAMP4 to generate fixed values of voltage in each one of the outputs of the analog demultiplex and measuring the values effectively generated by the circuit. Our calibration was done by linear fitting of the plot of the voltage found experimentally as a function of the different fixed voltages used (range between -10.0 and +10.0V).

The multiplexing of the four voltage commands in the two outputs of the DAC board is done by the DYNCLAMP4 as described in Figure 2. We used a hardware characteristic of the Digidata 1200A board that allows to write simultaneously to an analog output and to some of the digital outputs. The DAC in the board uses the 12 most significant bits of a 16 bits word and the 4 least significant bits of the word go to the bits D0 to D3 of the digital output. In this way when DYNCLAMP4 writes the digital value of the voltage corresponding to the current I1 to be converted to analog by the DAC it also writes a bit 1 in the digital output D0 and resets to 0 the other 3 digital outputs. At this time the sample and hold circuit of the analog demultiplex samples the CH0 output of the DAC (that now is already stable) during 15µs and generates the current I0. In the sequence, I2 will be written to CH0 output and a logical level 1 will be generated in D1, so I1 will be generated from the sampling of CH1. These procedure is repeated until all the commands are generated.

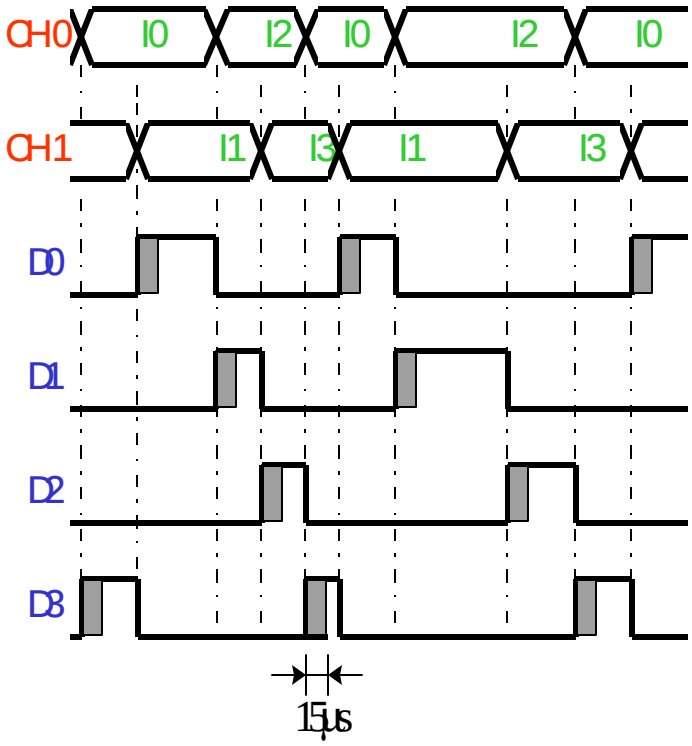

Figure 2. Temporal diagram of the control and analog signals in the analog demultiplex. The analog output CH0 (CH1) of the DAC board is used to sample the output voltages correspondent to the currents I0 and I2 (I1 and I3) to be injected in the cells 0 and 2 (1 and 3) respectively. Since the dynamic clamp cycle is asynchronous, the length of the control pulses (D0 - D3), generated simultaneously with the update of CH0 and CH1, is not constant. The sample signals to each sample and hold unit are generated by monostable TTL circuits (U3 and U4 in the previous figure) during a period of 15µs as shown by the marked regions.

We used coaxial cables to connect the Digidata analog and digital outputs to the analog demultiplex. The circuit was assembled inside a metallic grounded box were we used BNC connectors for connecting the analog demultiplex inputs to the Digidata board, and its outputs to the microelectrode amplifiers.

HOW TO INSTALL THE PROGRAMS:

First thing one need to do is to copy the driver file: Ioport.sys into the drivers directory of Windows. In Windows NT it is generally C:\Winnt\system32\drivers. Then, to choose which version is more suitable for its purposes, the DYNCLAMP2 or the DYNCLAMP4. Once made the decision one should unzip the corresponding file (DynClmp2.zip or DynClmp4.zip). Following is the description of the files contained in the zip files DynClmpX.zip:

- DynClmpX.exe: Is the only file one need to run the program (after copying Ioport.sys to the Windows drivers directory). Simply copy it to the directory you want and run it by clicking over the icon as usual;
- *.bpr, *.res, *.tds, *.cpp, *.h, *.dfm: Files with the source code, the visual project, and information that one need to modify or to recompile the program. Some of the files have the same name in the versions DYNCLAMP2 and DYNCLAMP4, so if you are going to unzip both versions we recommend to use different directories.

If one wants to modify or to recompile the program, Borland C++ Builder 4 or newer is required. One also will need to download and install in the C++ Builder software the IOport software component driver from Cybermagic Productions Ltd. to enable the access to the input/output hardware ports of the ADC/DAC board using C++ Builder. This component can be found in the web site: http://www.cybermagic.co.nz/winsoft/products.htm. Once installed the C++ Builder component just click over DynClmpX.bpr to open the Borland C++ Builder project.

IF THE DYNCLAMP WINDOW DOESN'T SHOW UP:

If you install DynClamp2 or DynClamp4 following the instructions above and when you run the program nothing appears in the screen but the task manager says the program is running and using a lot of CPU time it is probably because you have an I/O conflict of addresses between your DIGIDATA Board and some other computer hardware device. This can happen even if the DIGIDATA board works fine with Axon programs like Axoscope.

This problem happens because DynClamp needs to read the Real Time Counter (RTC) in the Digidata board that is never read by most Axon programs. Usually the DIGIDATA board

is configured to use the I/O address $320, and in this case the RTC reading ports are in the range $330 - $332. Many computers use the address $330 for some devices like sound cards, etc... And when you run DynClamp it freezes the program because the RTC cannot be reset.

How to diagnose and solve the I/O conflict?

Windows NT, 2000:

Open: Start -> Programs -> Administrative Tools -> Windows NT Diagnostics. Choose the folder <Resources>, click in <I/O Port> and use the cursor to browse the list of used ports. You should look for 330. Note that 320 will not appear because the Digidata Board is not detected by Windows. If you find any reference in the range 330 - 33F and your Digidata board is configured to use the base address 320 you need to change I/O address of your Digidata board to run DynClamp and avoid other problems due to the I/O conflict.

Windows 95, 98:

Open: Start -> Settings -> Control Panel -> System. Choose the folder <Device Manager>, click <I/O Port> and use the cursor to browse the list of used ports. You should look for 330. Note that 320 will not appear because the Digidata Board is not detected by Windows. If you find any reference in the range 330 - 33F and your Digidata board is configured to use the base address 320 you need to change I/O address of your Digidata board to run DynClamp and avoid other problems due to the I/O conflict.

Changing the base address of the Digidata Board and in the DynClamp programs:

You should look carefully for some free space in the list of port addresses, if 330 is been used, usually there is a lot of space around 340-370 that's enough for the whole Digidata board ports. Reconfigure manualy the Digidata board for the base address 340 or 350 (the RTC will be 350 or 360 and no conflicts!) and run the DynClamp program. The control screen will appear with the default Digidata base address 320 and you should change it to 340 or 350 (or whatever you have configured in your board) and click <change address>. The program will find the board and signalize it in the screen.

RUNNING DYNCLAMP4 OR DYNCLAMP2:

“Connecting” the program to the cells:

We encourage the insertion of two electrodes into each cell (or a careful impedance compensation of a single electrode) to avoid the generation of a wrong current command due to any artifacts produced by the current injection in the membrane potential signal.

If you are going to run DYNCLAMP2, the membrane potential output of the microelectrode amplifiers should be connected to the analog inputs 0 and 1 of the Digidata board. The command voltage for the injection of current into the cells will be in the analog outputs 0 and 1 respectively and should be connected to the current command input of the microelectrode amplifiers.

Running DYNCLAMP4 requires the use of the analog demultiplex and different connections. The membrane potential output of up to 4 cells should be connected directly to the analog inputs 0 to 3 of the Digidata board. The digital outputs 0 to 3 of the Digidata board should be connected to the inputs D0 to D3 of the analog demultiplex. The command voltage for injection of current will be in the outputs I0 to I3 of the analog demultiplex and should be connected to the current command input of the respective microelectrode amplifiers.

In both versions of the program, the currents are calculated individually for each conductance and synapse and then they are summed for each cell to generate the corresponding voltage command for the microelectrode amplifiers. A recommended procedure is before turning on the injection of the current in the microelectrode amplifier, to turn on the dynamic clamp cycle and to monitor the current command voltage in an oscilloscope to see if it looks like what is expected and if its value is not too big, avoiding damaging the cell due to mistakes when choosing parameters or any hardware misconfiguration.

Control Panel of the Program:

The control panel of the program can be divided in four different regions, one of them correspond to the configuration of the hardware and program control and the other three correspond to sets of similar blocks for controlling each individual electrical synapse, chemical synapse or conductance being simulated by the program. The panel was designed to allow the experimenter to control and to check the value of the parameters used in all the synapses and conductances in a single window, as well as indicates which are the synapses and conductances activated at a given moment.

To change a numeric value in a field one should click the mouse of the computer over the field and edit the value using the keyboard. There is no need to press Enter after editing the values. New values will only take effect when the main button Start/Update is pressed (with exception of the Digidata Board Address field that can be changed by its respective button).

Configuration of the Hardware and Control of the Program:

Once you run the program you can identify in the upper right corner of the control panel the block shown in Figure 3. The only difference concerning this block in the versions DYNCLAMP2 or DYNCLAMP4 is the number of channels available for configuration, respectively two or four channels. These upper labels, Ch_0, Ch_1, Ch_2, and Ch_3, indicate to which channel correspond the configuration fields.

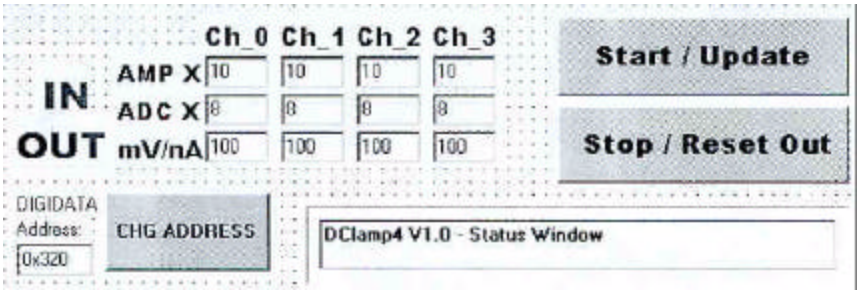

Figure 3. Configuration of the hardware and the control of the dynamic clamp cycle in the control panel of DYNCLAMP4.

If everything is OK the status window should show that the Digidata board was found. If it says "Digidata board not found" you should check if there is a Digidata board properly connected and working in the computer and, if positive, you should try another hardware address for the board. DYNCLAMP2 and DYNCLAMP4 default address for the board is 0x320 (hexadecimal), which is the default address of the board, but the specific board can have been configured to use another range of addresses. Possible values are 0x340, 0x360, 0x380, 0x3A0, 0x3C0, etc.

- **CHG ADDRESS**: button used to change the hardware address of the Digidata board. A new hexadecimal value should be typed in the corresponding field before pressing this button. When the board is found the Status Window will display the respective message.

- **AMP X**: field that indicates the gain factor of the microelectrode amplifier connected to the channel X. To change the default value click in the field containing the address and edit the value using the keyboard.

- **ADC X**: configures the input gain of the ADC channel X in the Digidata board. It is related to the precision of the A/D conversion and should be selected as big as possible. Allowed values for this parameter are: 8, 4, 2, 1, respectively corresponding to the ranges of input voltages -1.25V to +1.25V, -2.5V to +2.5V, -5.0V to + 5.0V, and -10.0V to +10.0V.

- **mV/nA**: correspond to the calibration of the current input command voltage in the microelectrode amplifiers in mV/nA for each channel. Since the range of the current voltage command output is -10V to +10V, one can select a higher ratio mv/nA and use a divider to match it to the input of the microelectrode amplifier, increasing the precision of the current generation.

- **Start/Update**: button that initializes the internal variables with the parameters found in the control panel and starts the dynamic clamp cycle. The parameters used in the synapses and

conductances can be changed in the control panel during the running of the program, but the changes will only modify the internal parameters responsible for the currents being generated after one press Start/Update.

- **Stop/Reset**: button used to stop the dynamic clamp cycle and to generate null currents in all the outputs.

The Status Window changes its color to indicate if the dynamic clamp cycle is active or not. The field that indicates the name of each synapse or conductance also change its color during the time the dynamic clamp cycle is running to indicate that the particular synapse or conductance is active and is being considered in the generation of the currents.

When using DYNCLAMP4 one should first press Stop/Reset to initialize the analog demultiplex avoiding the drift of the inactive sample and hold circuit to generate hyperpolarizing currents for the cells.

Electrical synapses:

Figure 4 shows the control block of an electrical synapse. The program DYNCLAMP4 has 6 of these blocks, corresponding to all the possible single electrical synapses each neuron can have with the others. The name of the block Elec X=Y means the synapse is between the cells corresponding to the channels X and Y. DYNCLAMP2 has two electrical synapses between the same pair of cells to allow some design of non-symmetric electrical synapse using rectification.

During the cycle of dynamic clamp if an electrical synapse Elec X=Y is active, the currents I_X and I_Y to be injected in the cells X and Y, respectively, are calculated according to:

$$I_Y(t) = G\_e[V_X(t) - V_Y(t)],$$

$$\text{and } I_X(t) = -I_Y(t).,$$

were V_x (t) and $V_Y(t)$ are the membrane potential of the cells X and Y respectively.

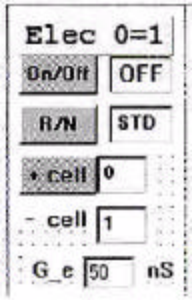

Figure 4. Control block for an electrical synapse between the cells corresponding to the channels 0 and 1 in DYNCLAMP2 and DYNCLAMP4.

- **On/Off**: button used to turn on or off each electrical synapse.

- **R/N**: button used to change the synapse from normal (STD) to rectifier (REC). If rectifier synapse is chosen, the current will be null unless the membrane potential of the cell defined as positive is at an higher level than the membrane potential of the cell defined as negative.

- **+ cell**: button that changes the polarity of the cells. It only produces any effect in the current if the synapse is set as rectifier.

- **G_e**: total conductance of the electrical synapse in nS (nano Siemens).

Chemical Synapses:

The control block of a chemical synapse is shown in Figure 5. DYNCLAMP4 has 12 of these blocks, corresponding to all the possible combinations of presynaptic and postsynaptic cells allowed to four neurons. The name of the block Chem X=<Y means the synapse is between the cells corresponding to the channels X and Y. The current to be injected in the postsynaptic cell Y is calculated according to the membrane potential of the presynaptic cell X. DYNCLAMP2 has two chemical synapses for each pair of presynaptic and postsynaptic cells, allowing one to play with the characteristic time constants and reversal potentials to simulate the effect of biphasic synapses.

During the cycle of dynamic clamp if a chemical synapse Chem X=<Y is active, the membrane potentials of the cells X and Y, respectively Vx and Vy are used to compute the current I_Y to be injected in the postsynaptic cell Y. I_Y is calculated using a first order kinetics model of the release of neurotransmitter (Destexhe *et al.*, *Neural Comp.* **6**, 14, 1994) and an additional inactivation term (h(t)) to simulate depression:

$$I_Y = G\_s \cdot S(t) \cdot h(t) \cdot [V\_s - Vy(t)],$$

where the instantaneous activation, S(t), and inactivation, h(t), terms are given by the differential equations

$$\left(1 - S_\infty(Vx)\right) Tau\_s \frac{dS(t)}{dt} = \left(S_\infty(Vx) - S(t)\right),$$

$$t_h(Vx) \frac{dh(t)}{dt} = h_\infty(Vx) - h(t),$$

where

$$S_\infty(Vx) = \tanh\left[\frac{Vx(t) - V\_th}{V\_sl}\right] \text{ when } Vx > V\_th,$$

$$\text{otherwise } S_\infty(Vx) = 0,$$

$$h_{\infty}(Vx) = \frac{a}{1+\exp\left(\frac{Vx - V\_th}{V\_sl}\right)}, \quad t_h(Vx) = Tau\_0 - \frac{a\_T}{1+\exp\left(\frac{Vx - Vth\_T}{Vsl\_T}\right)}.$$

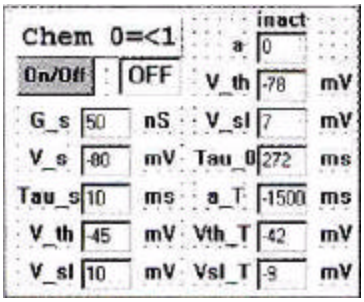

Figure 5. Control block for a chemical synapse between the presynaptic cell (channel 0) and the postsynaptic cell (channel 1) in DYNCLAMP2 and DYNCLAMP4.

- **On/Off**: button used to turn on or off each chemical synapse.
- **G_s**: maximum conductance of the chemical synapse in nS.
- **V_s**: reversal potential in mV.

activation S(t):

- **Tau_s**: synaptic characteristic time constant in msec.
- **V_th**: threshold potential for the release of neurotransmitter in mV.
- **V_sl**: slope voltage in mV.

inactivation h(t):

- **a**: 0→synapse without depression, 1→synapse with depression.
- **V_th**: threshold potential for the inactivation in mV.
- **V_sl**: inactivation slope voltage in mV.
- **Tau_0**, **a_T**, **Vth_T**, and **Vsl_T**: parameters for the inactivation characteristic time.

Hodgkin-Huxley Type Conductances:

Both DYNCLAMP2 and DYNCLAMP4 provide eight Hodgkin-Huxley type conductances that can be individually configured. This permits all the eight conductances to be inserted in a single cell or any other desired combination. The control block of a Hodgkin-Huxley type conductance is shown in Figure 6. The current (I_{HH}) to be injected in the cell with membrane potential given by V(t) is calculated using representations of the activation (m(t)) and inactivation (h(t)) of the conductance according to

$$I_{HH} = Gmax \cdot m^p(t) \cdot h^q(t) \cdot (E_r - V(t)),$$

where m and h are modeled as

$$t_m(V)\frac{dm}{dt} = m_\infty(V) - m,$$

$$t_h(V)\frac{dh}{dt} = h_\infty(V) - h,$$

$$m_\infty, h_\infty = \frac{a}{1+\exp\left(\frac{V - V\_th}{V\_sl}\right)},$$

$$t_m, t_h = Tau\_0 - \frac{a\_T}{1+\exp\left(\frac{V - Vth\_T}{Vsl\_T}\right)},$$

where we represented the expressions for m_∞, h_∞ , and τ_m, τ_h sharing the same parameters for simplicity, but these parameters are individually configured for the activation and inactivation in the control block of the conductance.

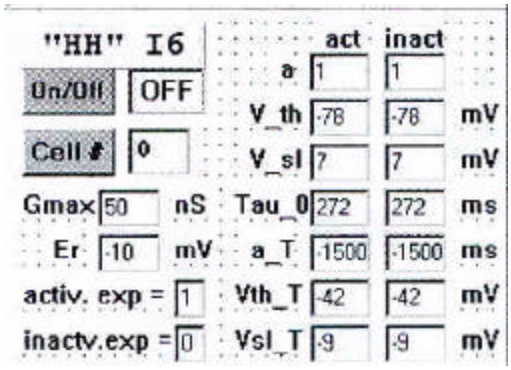

Figure 6. Control block of a Hodgkin-Huxley type conductance in DYNCLAMP2 and DYNCLAMP4.

- **On/Off**: button used to turn on or off each Hodgkin-Huxley type conductance.
- **Cell #**: button used to change the channel in which the conductance is inserted.
- **Gmax**: maximum value of the conductance in nS.
- **Er**: reversal potential in mV.
- **activ. exp**: exponent of the activation term m(t).
- **inactv. exp**: exponent of the inactivation term h(t).

Activation/Inactivation parameters:

- **a**: should be left in 1 since one can turn off the activation/inactivation setting the respective exponent = 0.
- **V_th**: threshold potential in mV.
- **V_sl**: slope voltage in mV.
- **Tau_0**, **a_T**, **Vth_T**, Vsl_T: parameters that define the timing of activation or inactivation.

USER FEEDBACK:

This is the first effort to write some documentation about the program, so it can be not completely clear sometimes... Any comments or questions to improve this document or about the operation of the program are very welcome and can be send to the main author: reynaldo@ucsd.edu or reynaldo@fge.if.usp.br. If you change the code, please send me the alterations you did and a short explanation, so I can update the program in the web site.

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RDP 08/16/2001